

LEADING FUTURE ELECTRONICS INTO THE NANO REGIME USING QUANTUM ATOMISTIC SIMULATIONS IN NEMO5

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EXECUTIVE SUMMARY

With a revenue of \$338.9 billion in 2016, and as an enabler for larger economy chains (i.e., electronic systems), the semiconductor industry influences approximately 10% of the world GDP [1]. The transistor is at the heart of this enormous industry and continuous improvements of transistors in terms of speed and power consumption are essential for the stability and growth of the semiconductor industry as well as the dependent product chains and economies. Needed improvements in transistors' performance have driven the semiconductor industry to push for smaller transistors, reaching 14 nanometers (nm) in the latest technology mode, while development is ongoing for 10 nm technology and beyond. Such aggressive downscaling into a countable number of atoms in the critical dimensions makes atomistic simulations necessary pathfinders in the quantum regime. NEMO5 is designed to comprehend the critical multiscale, multi-physics phenomena for nano-scale technology through efficient computational approaches, and enables quantitative study of new generations of nano-electronic devices even beyond transistors [2–3].

RESEARCH CHALLENGE

The U.S. has always been a world leader in the semiconductor industry with 40% of the worldwide semiconductor device-related patents originating in the U.S [4]. The U.S. semiconductor industry is one of the nation's largest and most strategic industries, and the U.S. holds one-third of the global semiconductor device market worth over \$300 billion per year. Simultaneously, a relentless downscaling is occurring, with devices expected to be about 5 nm long in their critical active region within 10 years. Further

improvements in shrinking dimensions will come only through the detailed study of device designs, materials, and of quantum effects such as tunneling, state quantization, and atomistic disorder. Fundamental questions remain about the downscaling of the CMOS (complementary metal-oxide-semiconductor) switch and its eventual replacement. What is the influence of atomistic local disorder from alloy, line-edge roughness, dopant placement, and fringe electric fields? How do lattice distortions due to strain affect carrier transport in nanometer-scale semiconductor devices such as nanowires, finFETs, quantum dots, and impurity arrays? What are the effects of interconnects' sidewall roughness, grain boundaries, electron-phonon scattering, and roughness of metal-dielectric interfaces? Can inserting new materials and device concepts reduce power consumption?

NEMO5 is developed and used by the Institute for NanoElectronic Modelling (iNEMO) at Purdue University to address these fundamental questions on a variety of semiconductor devices. Besides enabling basic engineering, physics, and materials science research, NEMO5 is used by leading semiconductor firms to design future devices. The source code, binaries, and support for academic use are available through nanoHUB.org.

METHODS & CODES

iNEMO's research on Blue Waters encompasses multi-physics atomistic quantum simulations implemented in NEMO5. The needed physics vary from one device to another, but all can be simulated inside NEMO5. Several examples follow: For transistors, quantum transport simulations are performed using the self-consistent Poisson with nonequilibrium Green's function (NEGF)

approach employing semi-empirical tight binding methods. The current mechanism of tunneling field effect transistors (TFETs) is through inter-band tunneling rather than thermionic emission in typical MOSFETs (metal-oxide semiconductor field-effect transistors). For realistic performance predictions, incoherent scattering effects are also included.

For nitride devices, namely nitride-based light emitting diodes and alloy engineered Nitride TFETs, a multi-scale quantum transport model is used, which treats high-density regions as local charge reservoirs, where each reservoir serves as carrier injector/receptor to the next/previous reservoir.

RESULTS & IMPACT

For nitride devices, the I–V characteristics produced from these simulations agree quantitatively with experimental measurements. The simulations have been used to suggest improvements in the multi-quantum-well nitride-based light-emitting diode. In addition to this, a new alloy engineered Nitride TFET is proposed as a novel low-power transistor design.

Regarding transistor simulations, the tunneling from the valence to conduction band has the potential to yield significantly improved subthreshold slopes to allow lower supply voltages and much-needed lower power consumption compared to MOSFETs. Electron transport through the overall device, including the source and drain, entails significant amounts of computationally demanding scattering, which cannot be ignored in realistic device performance predictions. A new method on the rank reduction of matrices through basis transformations that retain key physical information for modeling incoherent scattering phenomena has been implemented in NEMO5. These low-rank approximations provide shorter times-to-solution and smaller memory footprints. Blue Waters was used for assessing these times-to-solution and memory improvements. Using these low-rank approximations on nano-wire with a width of 5 nm shows a speed-up of 200 and needs only 7% of the memory.

WHY BLUE WATERS

Quantum transport simulations are very computationally expensive and memory demanding due to the high degree of complexity of the equations used, especially if incoherent scattering of particles is needed. A toy quantum transport calculation of a 50 nm long wire with a 3 nm diameter requires around 1 teraflop for a single energy point where more than 1,000 energy points are needed. And this calculation must be repeated perhaps hundred times for a full current-voltage sweep. The treatment of a realistic device would require an atomistic resolution of a device with a cross section of more than (20x20) nm², which includes the core semiconductor and the surrounding gate material. Such devices of larger sizes are especially an issue due to the $O(n^3)$ scaling of matrix operation time-to-solution and $O(n^2)$ scaling of memory. Blue Waters was used for running such simulations on up to 16,384 cores per simulation. In many cases the work could not be accomplished in a reasonable amount of time without Blue Waters,

and for the larger simulations the work could not be accomplished on other available systems. Blue Waters staff provide exemplary support and user outreach to guide system usage, help with issues as they arise, and assistance with code performance and scaling.

PUBLICATIONS AND DATA SETS

Geng, J., et al., NEMO5: realistic and efficient NEGF simulations of GaN light-emitting diodes. Invited talk, *SPIE Photonics West OPTO 2017*, San Francisco, Calif., January 30–February 2, 2017.

Charles, J., et al., Non-Local Scattering with a New Recursive Nonequilibrium Green's Function Method. *IWCE 2017*, Windermere, United Kingdom, June 7–9, 2017.

Ilatikhameneh, H., T. Ameen, G. Klimeck, and R. Rahman, Universal behavior of atomistic strain in self-assembled quantum dots. *IEEE Journal of Quantum Electronics*, 52:7 (2016), pp. 1–8.

Huang, J., et al., Sb- and Al-Free Ultra-High-Current Tunnel FET Designs. *5th Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop*, Berkeley, Calif., October 19–20 2017.

Long, P., et al., A high-current InP-channel triple heterojunction tunnel transistor design. *75th Device Research Conference*, Notre Dame, Ind., June 25–28, 2017

Valencia, D., et al., Grain boundary resistance in nanoscale copper interconnections. *SISPAD 2016*, September 6–8, 2016.

Ameen, T., et al., Alloy Engineered Nitride Tunneling Field Effect Transistor: A Promising Energy Efficient Transistor. *TECHCON*, Austin, Texas, September 10–12, 2017.

Chen, C., et al., Channel thickness optimization for TFETs. *TECHCON*, Austin, Texas, September 10–12, 2017.

Sarangapani, P., et al., Non-equilibrium Greens function method: Band tail formation in non-local polar optical phonon scattering. *International Workshop on Computational Nanotechnology*, Windermere, U.K., June 5–9, 2017.

Sarangapani, P., et al., Non-equilibrium Green's function (NEGF) Approach: Phonon and Impurity Driven Band Tail Formation in Polar Materials. *TECHCON*, Austin, Texas, Sept. 10–12, 2017.

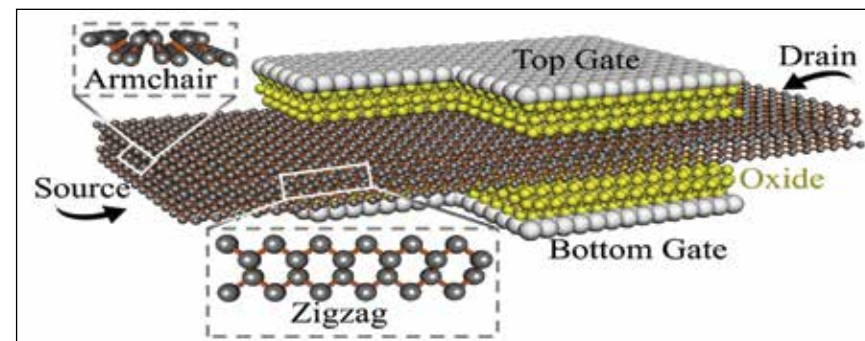


Figure 1: A 3D visualization of a typical sub-10 nm novel transistor design made from bilayer phosphorene that is being investigated using NEMO5. (Credit: Tarek Ameen)

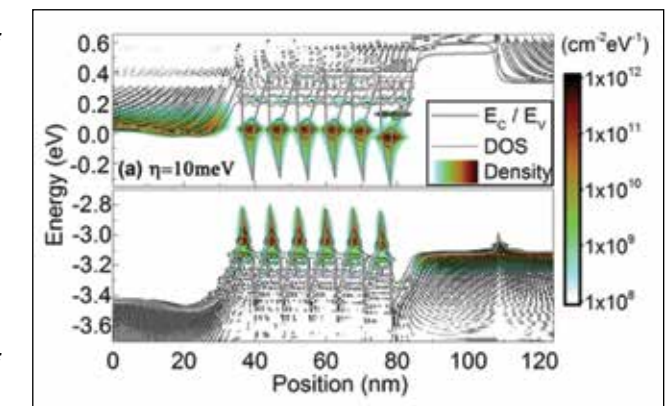


Figure 2: Energy-resolved electron, hole density of states (contour lines) filled with electrons and holes (color contours) of energy efficient multi-quantum well light-emitting diode simulated by NEMO5. (Credit: Junzhe Geng, Gerhard Klimeck)