Nanoelectronic Modeling on Blue Waters with NEMO5

NEMO5 software team:

Students: Tarek Ameen, James Charles, ChinYi Chen, Fan Chen, Yuanchen Chu, Rifat Ferdous, Junzhe Geng, **Xinchen Guo**, Yuling Hsueh, Hesam Ilatikhameneh, Pengyu Long, Daniel Lemus, Kai Miao, Daniel Mejia, Samik Mukherjee, Harshad Sahasrabudhe, Prasad Sarangapani, Frederico Severgnini, Archana Tankasala, Daniel Valencia, KuangChung Wang, Yu Wang, Evan Wilson

4 Professionals: Jun Huang, Tillmann Kubis, Bozidar Novakovic, Michael Povolotskyi

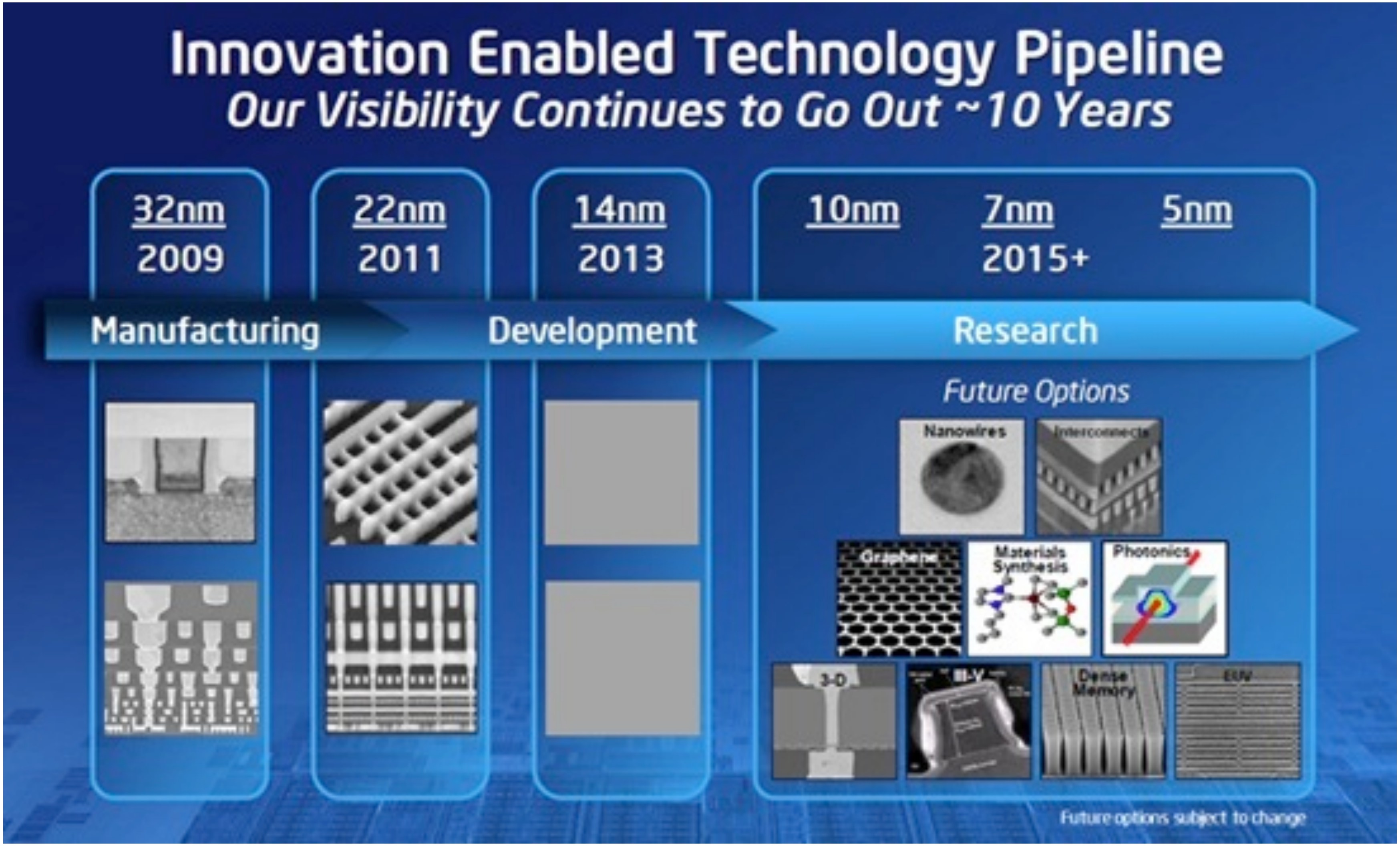
Supervision: Gerhard Klimeck

Network for Computational Nanotechnology (NCN)

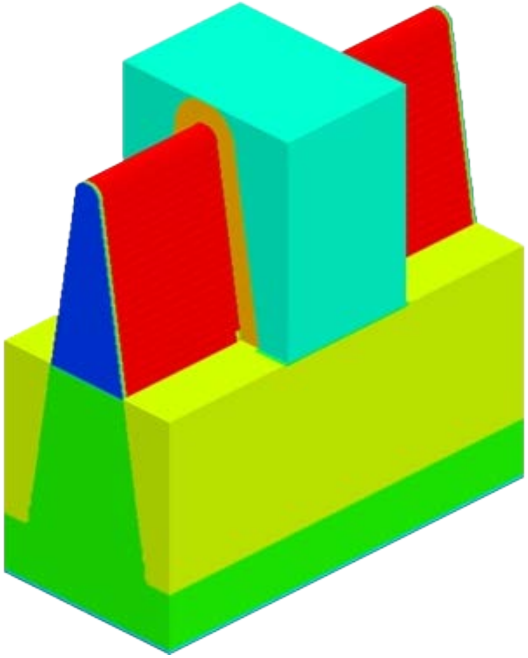
Electrical and Computer Engineering

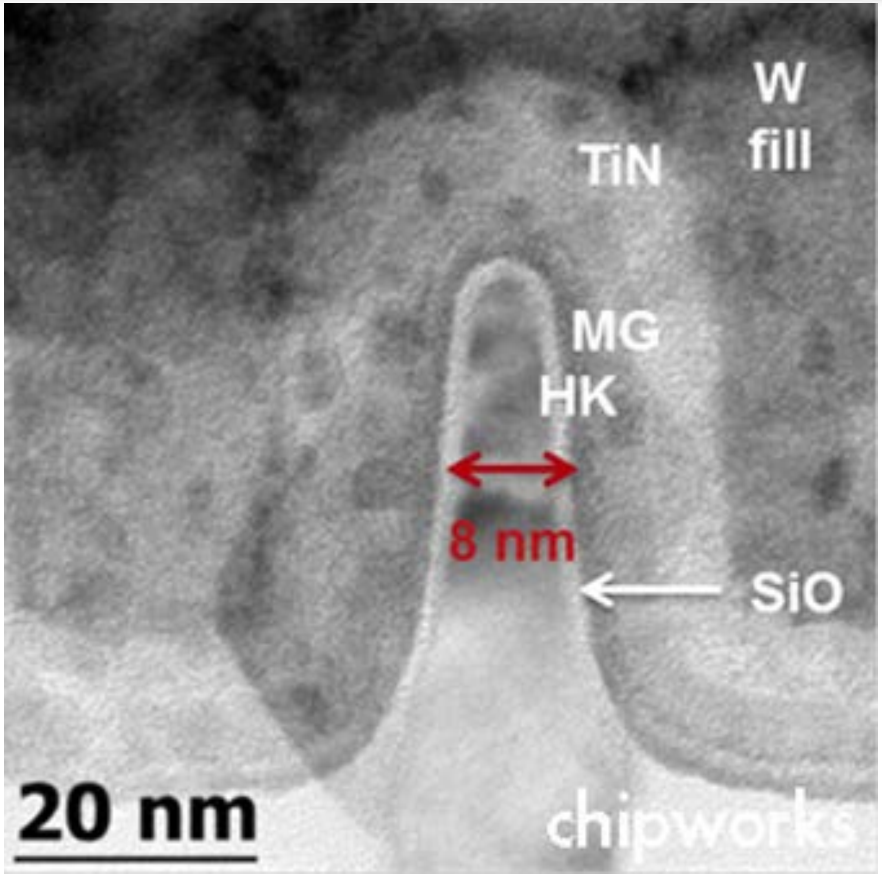
Outline

- NEMO5 and nanoHUB
- Science on Blue Waters
  - » Electron-phonon scattering
  - » Multi-quantum well LEDs
  - » Compact model for copper grain boundaries
  - » Flying qubit modeling
- Summary


Innovation Enabled Technology Pipeline
Our Visibility Continues to Go Out ~10 Years
32nm
2009
22nm
2011
14nm
2013
10nm
7nm
2015+
5nm
Manufacturing
Development
Research
Future Options
Nanowires
Interconnects
Graphene
Materials Synthesis
Photonics
3-D
III-V
Dense Memory
EUV
Future options subject to change

Nanoscale Atomistic Simulations
Intel 22nm FinFET Transistor



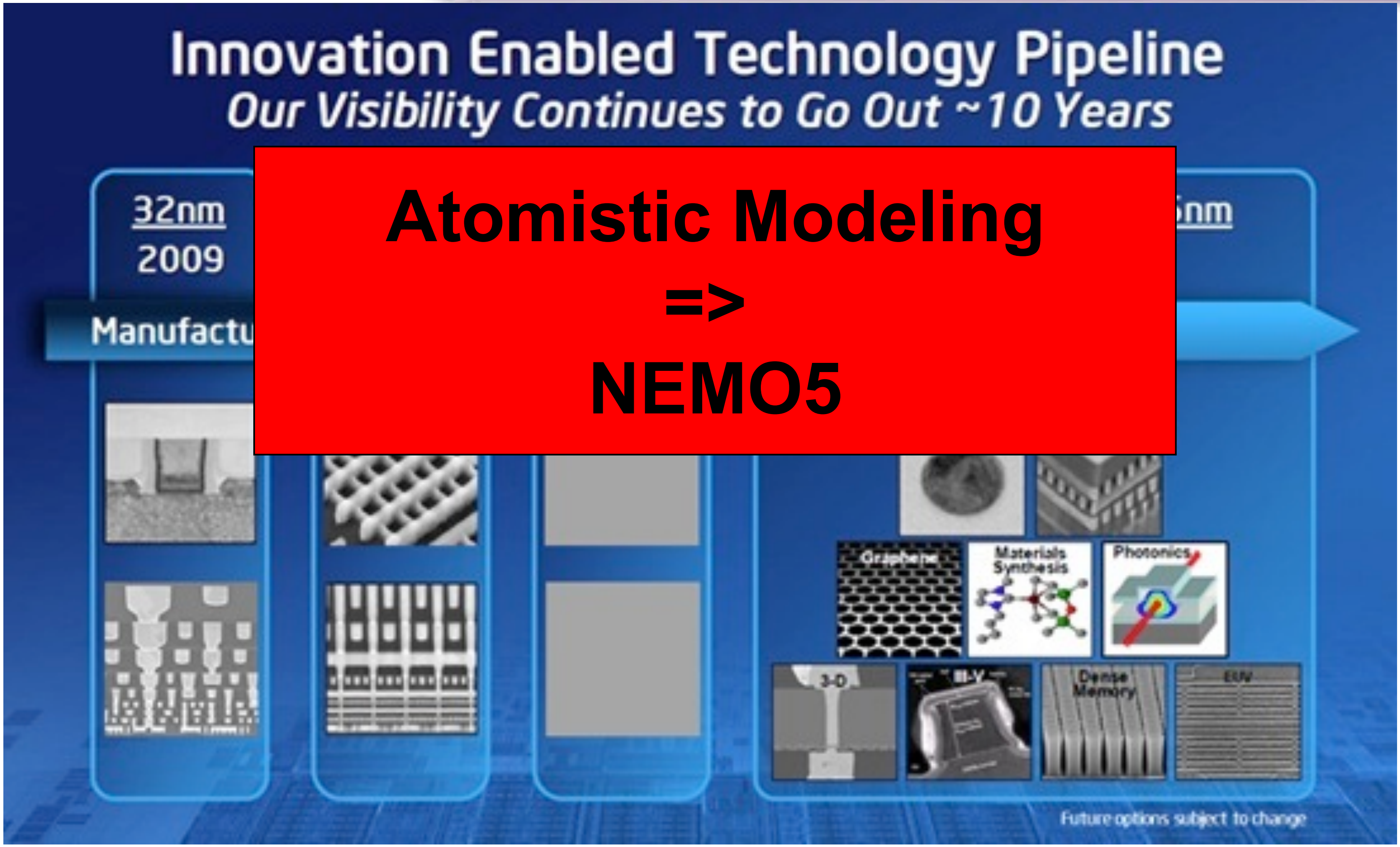


Gate length: 22nm = 176 atoms

Active region: 8nm = 64 atoms

http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/

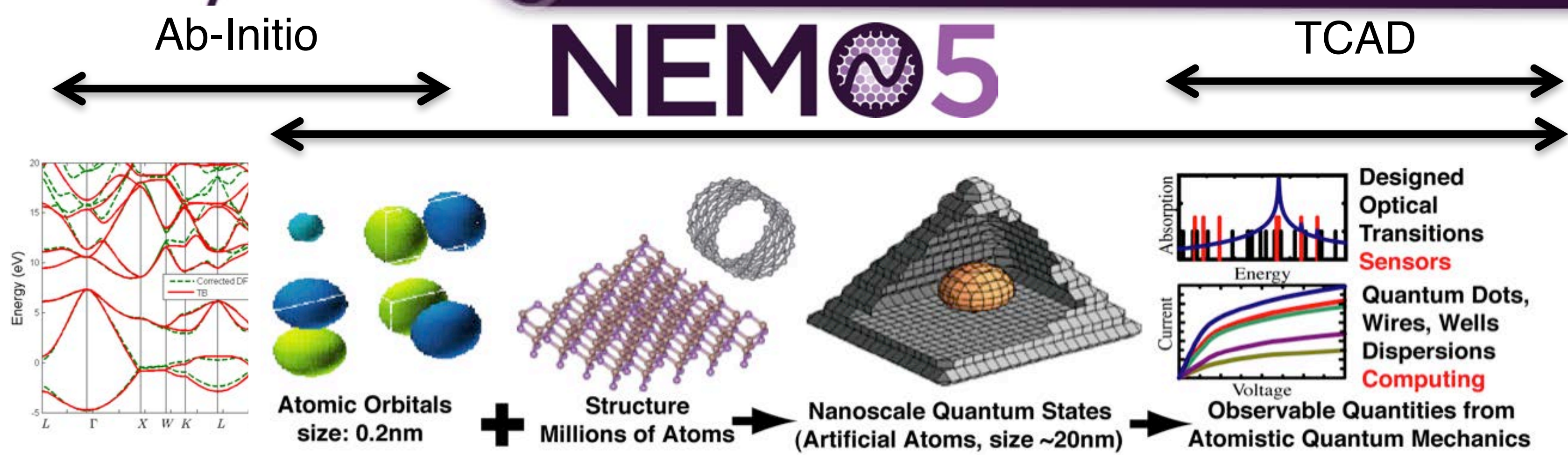
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

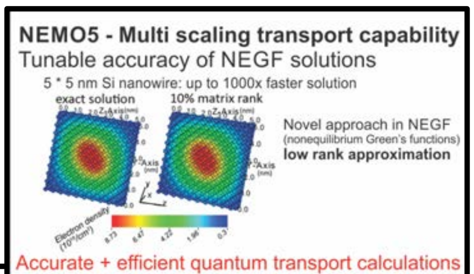


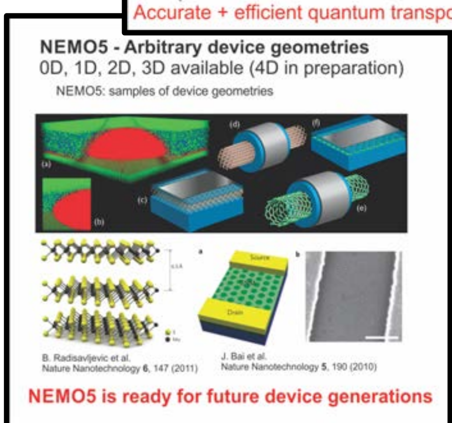
Atomistic Modeling
=>
NEMO5

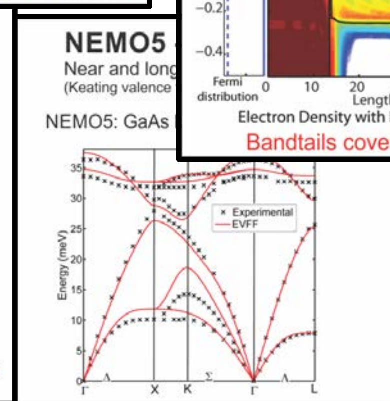
nm Node	22	14	10	7	5
Node atoms	176	122	80	56	40
Critical atoms	64	44(?)	29(?)	20(?)	14(?)
Electrons	160-190	64-80	30-38	18-23	11-15

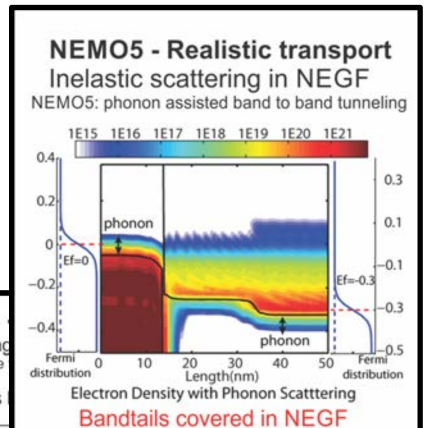
NEMO5 - Bridging the Scales From Ab-Initio to Realistic Devices

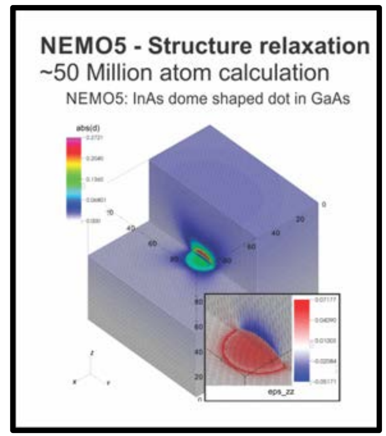


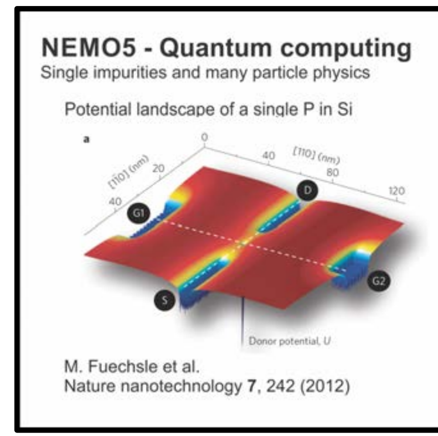












Multi-scale, multi-physics and multi-purpose nanotechnology simulation software

Broad Usage in Academia and Industry

Offline Applications

- Academia > 400 groups
- Intel
- Samsung
- TSMC
- Philips

Online Applications

- nanoHUB

Power **9** Tools: (By February, 2017)

23,874 users

465,509 simulation runs

381 classes w/ 3,756 students

88 citations

Large number of academic and industrial users worldwide

Broad Usage in Academia and Industry

Available NEMO5 configurations for CPU, GPU, Xeon Phi

```
                         (for Macs)
                         (gcc generic Kubuntu 10.04)
                         (gcc + MKL on fedora)
                         (gcc static build on ubuntu)
                         (build on ubuntu with Intel compilers
                         (                                   ds checks)
                         (
                         (                                   4)
carter-impi-petsc34-gpu-libs  (                              openmp)
carter-impi-petsc34-libs      (                              same as 'carter-impi-petsc34' but with group libraries)
carter-gcc-petsc34       (same as carter-impi-petsc34 but with GCC compiler for C/C++: Carter)
                   4-libs   (same as carter-gcc-petsc34 but uses libs in group's shared application space: Carter)
                         (same as 'carter-impi-petsc34' but with PETSc developmental version: Carter/Conte)
          gpu-openmp-libs (same as carter-impi-petsc34-libs but with OpemMP and GPU)
                         (Configuration with PETSc 3.4 built with GPU support using CUSP and CUSPARSE)
          bs             (same as carter-gcc-petsc34 but uses libs in group's shared application space: Conte)
          bs             (Use precompiled libraries on Conte. GCC 5.2.0, PETSc/SLEPc 3.5.4, LibMesh 0.9.5 in optimized mode)
          4              (Conte configuration compiled with Intel 14 compiler; used for MIC offload)
          4-libs                                             er with group libraries; used for MIC offload)
          4-hstrean                                          14 compiler with group libraries; used for MIC offload

          5                                                  n Intel 15)
          5-no-mic                                           n Intel 15, without Intel Xeon Phi support)
          5-no-mic-                                          with Intel 15, without Intel Xeon Phi support, with group

          5                                                  n Intel 16, required for hStreams)
                 (F                                          milar to Conte w/o MICs)
          -libs                                              ; similar to Conte w/o MICs)
                                                             and PETSc 3.5
                         (Rice configuration compiled with Intel 16 compiler and PETSc 3.7
          -libs          (Rice configuration compiled with Intel 16 compiler and PETSc 3.7
stampede                 (Stampede TACC
stampede-knl             (Stampede-KNL T
stampede-libs            (Stampede TACC
                              s sup
                              s sup
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                              s supercomputer with Intel and petsc34)
                              s supercomputer with Intel and petsc34)
                              s supercomputer with gcc
                              s supercomputer with gcc
                              eavour cluster with Xeon
                              SDSC)
                              supercomputer with inte
                              supercomputer )
                              supercomputer with intel
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BLUE WATERS

NEMO5 designed for compatibility with "any" system: from a PC to Tianhe-2

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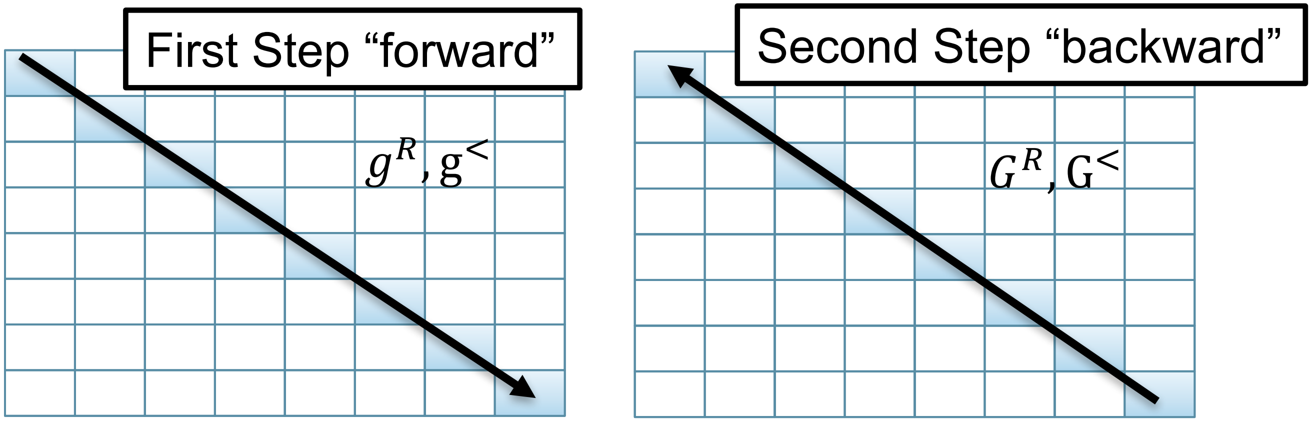
Electron-phonon Scattering State of Literature Solutions

Key equation: $(E - H - q\phi - \Sigma^R)G^R = I$
Solving G^R involves an inversion.

Status of literature:
Solve block diagonal Green's functions with either
- recursive Green's function method (RGF) -- not enough physics
- dense Green's function matrices ("full inversion") -- numerically unfeasible

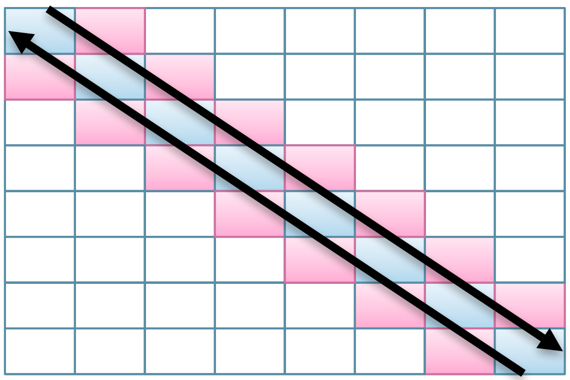
Typical RGF implementation:



Known RGF-algorithms are incompatible with nonlocal scattering

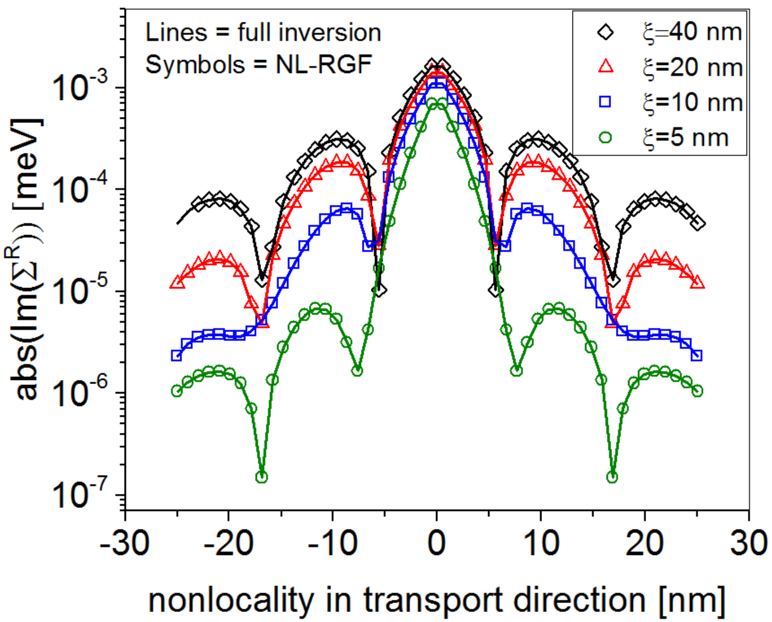
Electron-phonon Scattering Nonlocal RGF and Validation

Non-local RGF method:
Adding off-diagonal blocks



Bulk GaAs Tight binding $sp^3d^5s^*$
Polar optical phonon $\Sigma_{scatt}^{R/<}$ *

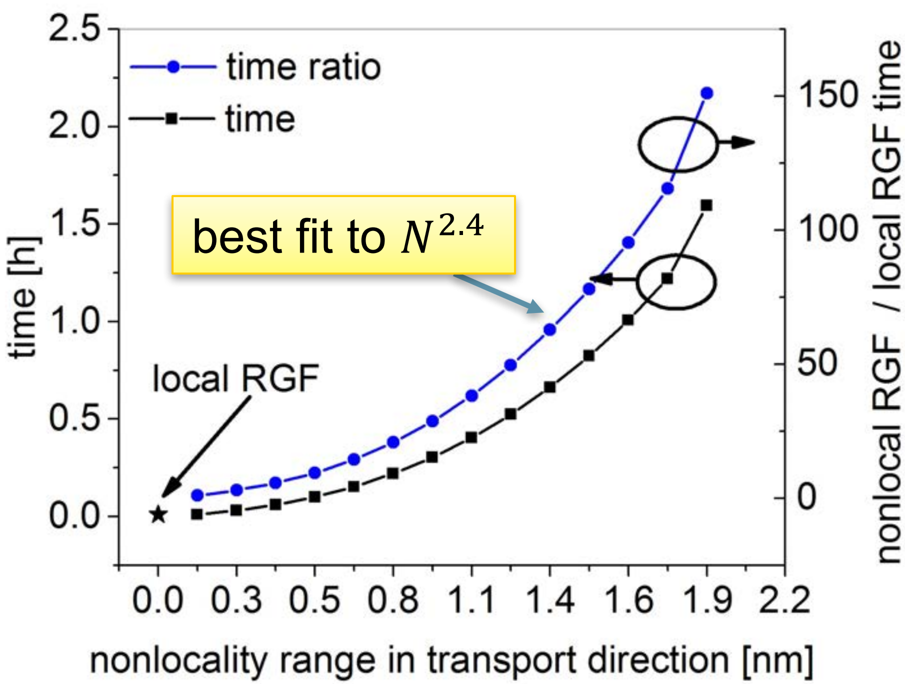
$\xi - screening\ length$

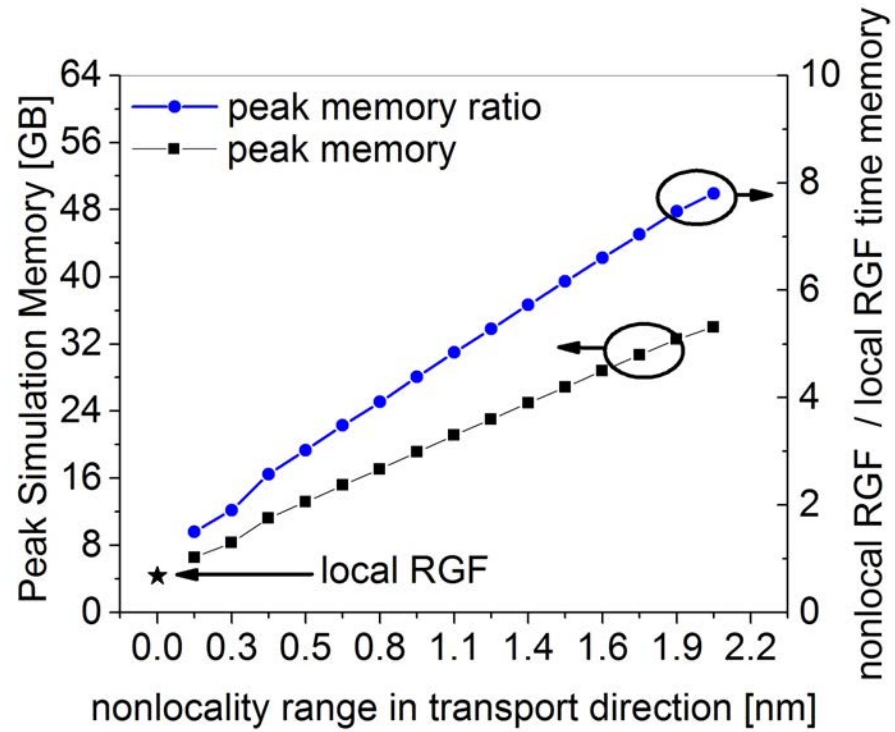


Non-local RGF produces accurate simulation result

Electron-phonon Scattering Nonlocal RGF Performance

2x2x20 nm wire in $sp^3d^5s^*$ – single energy point
Nonlocality -> number of off-diagonal blocks used





150 GB for one full matrix inversion

Nonlocal RGF is computationally expensive and memory consuming
Need 500 ~ 2000 nodes per simulation

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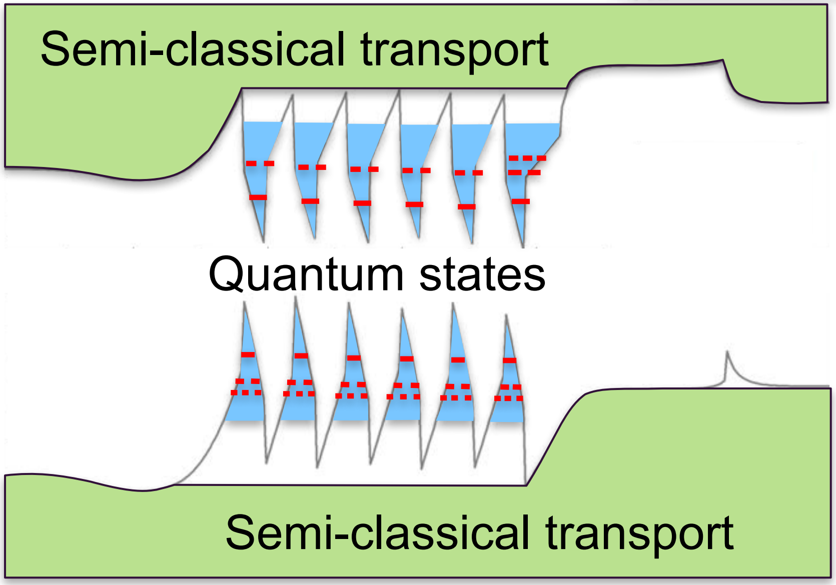
Multi-quantum Well LEDs
Classical Models Missing Key Information



Problems:
1. Semi-classical transport neglects:
   - Band structure details
   - Quantum effects
2. Distinction between continuum and discrete states is required

Solution: Self-consistent Non-Equilibrium Green's Function (NEGF) iterations

Quantum states:

Green's functions: $(E - H_0 - e\Phi - \Sigma^R)G^R = 1$

Distribution:

$G^< = G^R\Sigma^<G^{R\dagger}$

Self-consistent solution required!

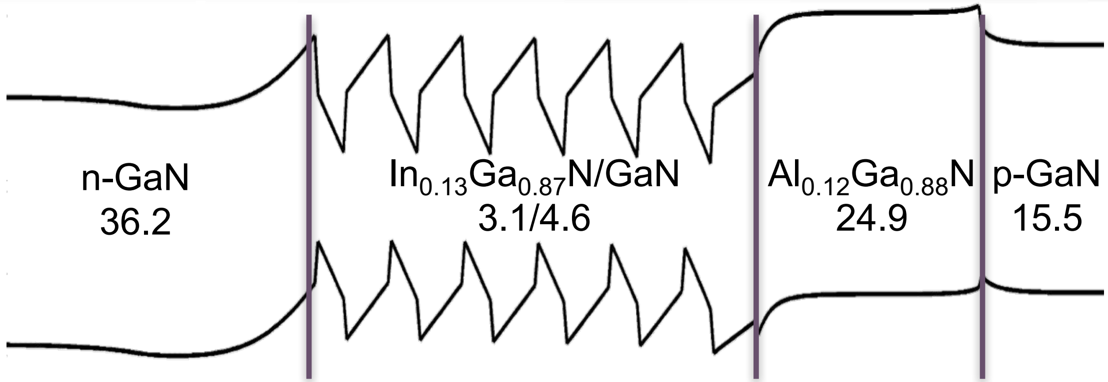
Self-energies $\Sigma^R = D^<G^R + D^RG^R + D^RG^<$

$\Sigma^< = D^<G^<$

Self-consistent NEGF is expensive for large LED devices

Multi-quantum Well LEDs Simulation Load: Single I-V

Typical Device Structure (Units in nm)



Simulation load:

- Simulation domain size: 123 nm (952 atoms)
- matrix size: ~ 19,000 by 19,000

Computation details:

- 10 bias points for each current-voltage (I-V) curve
- 100 nodes on Blue Waters for each bias point
- On average takes ~ 0.5 hour per job

Total simulation time for single I-V (10 points): 500 node hours

Multi-quantum Well LEDs Total Simulation Load

Calibrate physics parameters:

- 316 I-V curves
- 158,000 node hours

Sample production run:

- Sweep over various device structure parameters including barrier width, Indium concentration, Aluminum concentration, etc.
- Compare device performance over different designs
- 10~20 I-V curves for each parameter
- ~ 120 I-V curves in total
- ~ 60,000 node hours

Large amount of mid-size jobs need a large system to minimize turnaround time

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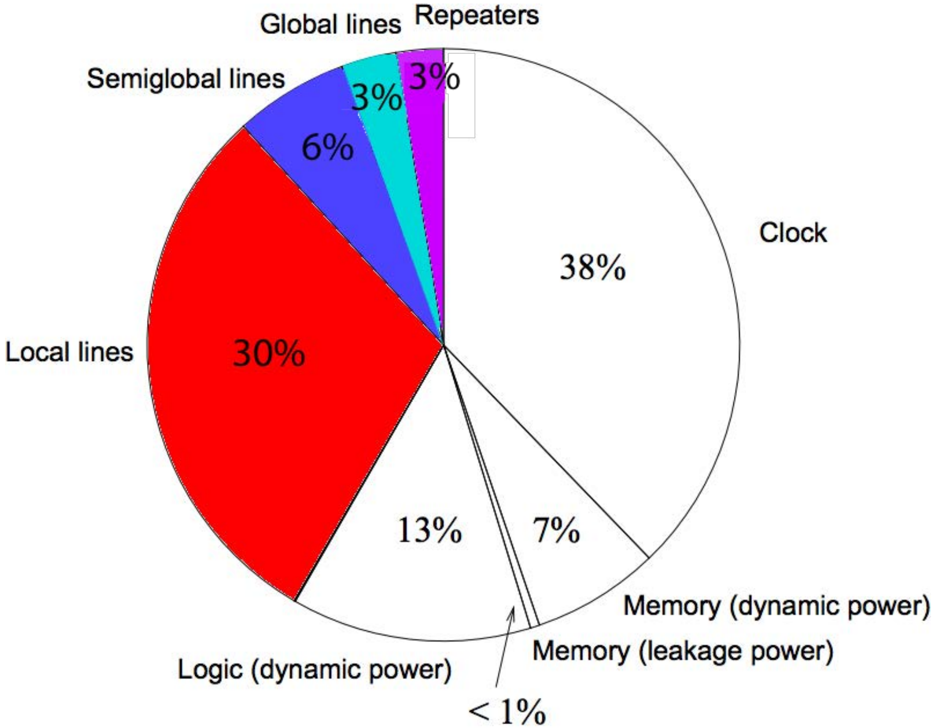
Compact Model for Cu Grain Boundaries Power Consumption of Cu Interconnects

Problem: Downscaling has reduced interconnect size, which has increased resistivity and static power consumption in electronic devices.

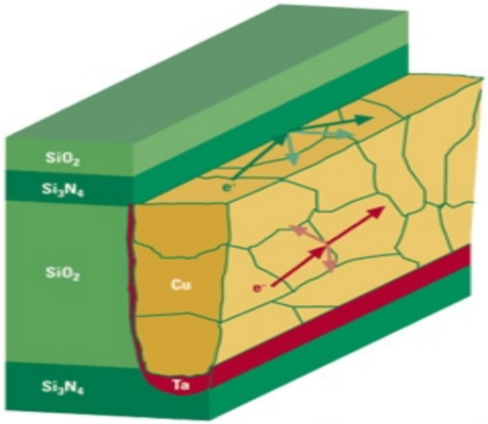
Power consumption 45nm node



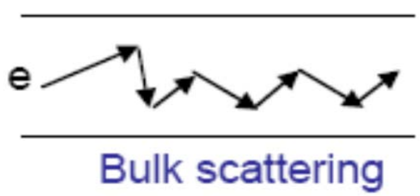
ITRS roadmap (2012)

Interconnects consume **over 42%** of the power in a modern chip**.**

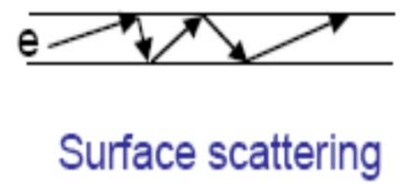
Copper Interconnects



Large Interconnects (linewidth >> 100 nm)



Short Interconnects (linewidth < 100 nm)



Grain boundary and surface roughness effects must be included at regimes where the interconnect size is small

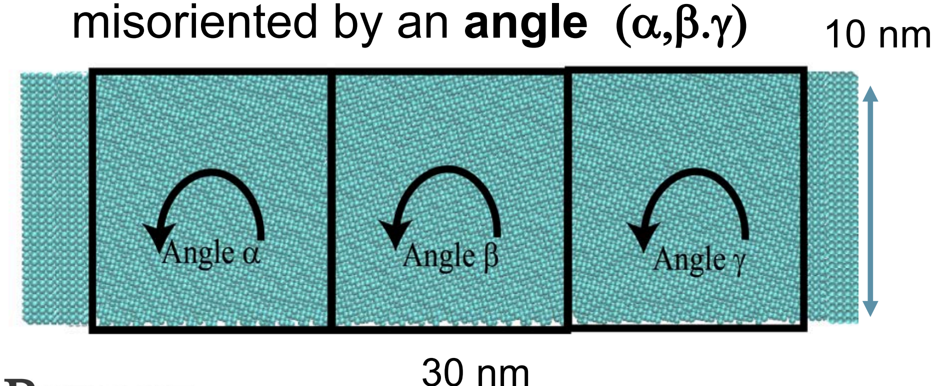
Compact Model for Cu Grain Boundaries Traditional Model and Why Blue Waters

Challenges of traditional model:

- Fail to describe the effect of surface roughness and grain boundary individually
- Use a pure fitting process and result in a lack of physical meaning of those parameters

Solution: Construct a grain boundary effects model based on atomistic model rather than pure fitting

Grain boundaries (GB) are created for relaxed copper interconnects misoriented by an **angle** (α,β.γ)



Computational requirements:

- ~ 800 samples to statistically describe the GB effects on copper interconnects as a function of the misorientation (α,β.γ)
- 3,520 FP cores (220 nodes) for 0.46h per sample
- ~ 100 node hours per sample
- ~ 80,000 node hours per interconnect structure
- Multiple interconnect structures needed for various transistor devices

Large amount of simulation hours needed for real engineering design

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Flying Qubit Modeling

Key challenges of qubits:

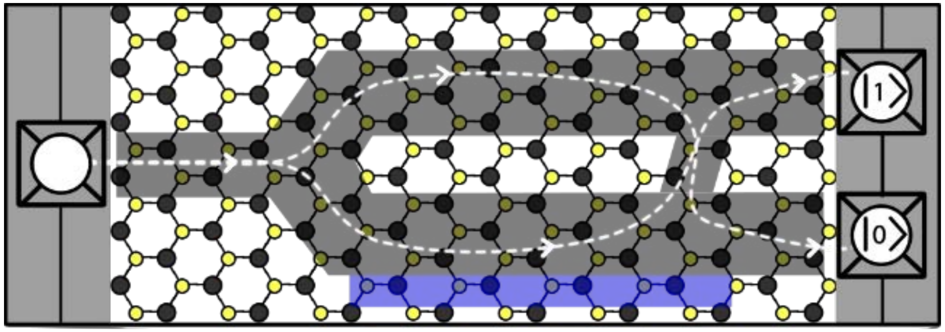
- Superconducting qubits scalable only to a handful of qubits[1]
- Semiconductor quantum dot qubits scalable[2], but suffer from decoherence upon reading[3]

Why it matters:

- A usable quantum computer requires millions of qubits[4] to allow for quantum error correction[5]

Our solution:

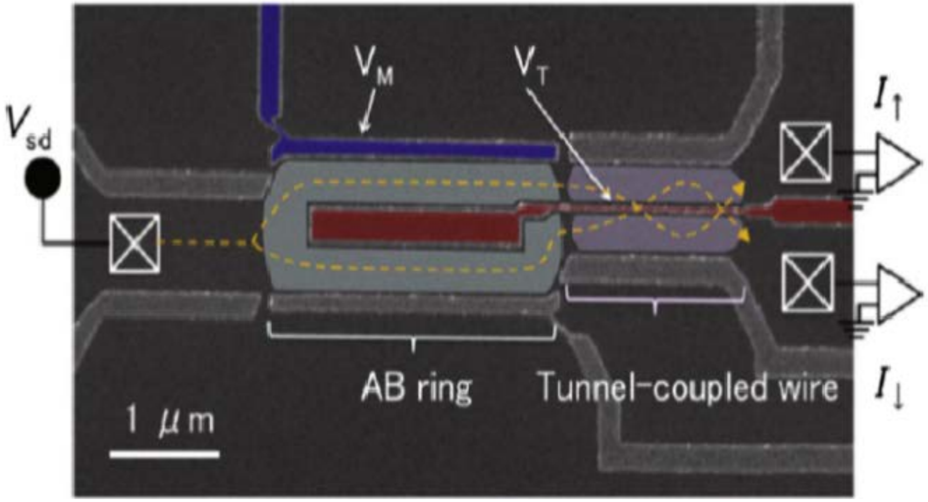
- Flying qubit -> electrons are moving vs stationary in quantum dots
- Use quantum transport to read qubit information with Mach-Zehnder interferometer[6] for minimal interference
- Qubit superposition controlled by gate (shown in blue)



Flying qubits are very promising for large scale quantum computers

[1] L. M. Vandersypen, M. Steffen, G. Breyta, I. L. Chuang et. al, Nature, vol. 414, no. 6866, pp. 883–7, 2001.
[2] I. L. Chuang, Q. Computation, R. Laflamme, J. I. Cirac, J. M. Raimond et. al, Science (80)., vol. 339, March, pp. 1174–1179, 2013.
[3] W. G. Van Der Wiel et. al, Rev. Mod. Phys., vol. 75, no. January, pp. 1–22, 2003.
[4] L. R. Schreiber and H. Bluhm, Nat. Nano., vol. 9, no. 12, pp. 966–968, 2014.
[5] T. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. O'Brien, Nature, vol. 464, no. 7285, pp. 45–53, 2010.
[6] T. Zibold, P. Vogl, and A. Bertoni,Phys. Rev. B - Condens. Matter Mater. P

Flying Qubit Modeling Simulation Requirements



AlGaAs/GaAs Interferometer device, taken from Ref 1.

Size limitations:

- **Micrometer** dimensions, very slow to model atomistically
- 2D device solutions allow control of decoherence[2,3] but require large dimensions of **tens or hundreds of nanometers**

Computational requirements:

- With basis reductions, each simulation expected to require 1,000 nodes for 40 hours, **40,000 node hours**
- ~ 20 simulations needed for various 2D materials/dimensions

Need 800,000 node hours with optimized algorithm

[1] S. Takada, M. Yamamoto, C. Bäuerle, S. Tarucha et. al, Appl. Phys. Lett., vol. 107, no. 6, 2015.
[2] M. Lundstrom and Z. Ren, IEEE Trans. Electron Devices, vol. 49, no. 1, pp. 133–141, 2002.
[3] C. Blömers, T. Schäpers, T. Richter, R. Calarco, H. Lüth, and M. Marso, Appl. Phys. Lett., vol. 92, no. 13, 2008.

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Summary

- NEMO5: multi-scale, multi-physics and multi-purpose nanotechnology simulation software
- Atomistic scale simulations are numerically expensive
- Blue Waters is necessary for:
  - » Large-size (~ 1000 nodes) jobs
    - ✓ Capability computing
    - ✓ Meet the minimum memory and cores requirements
    - ✓ non-local RGF, flying qubits, etc.
  - » Mid-size (~ 100 nodes) jobs
    - ✓ Capacity computing
    - ✓ Minimize the turnaround time of a large amount of simulations
    - ✓ LEDs, Cu interconnect, etc.