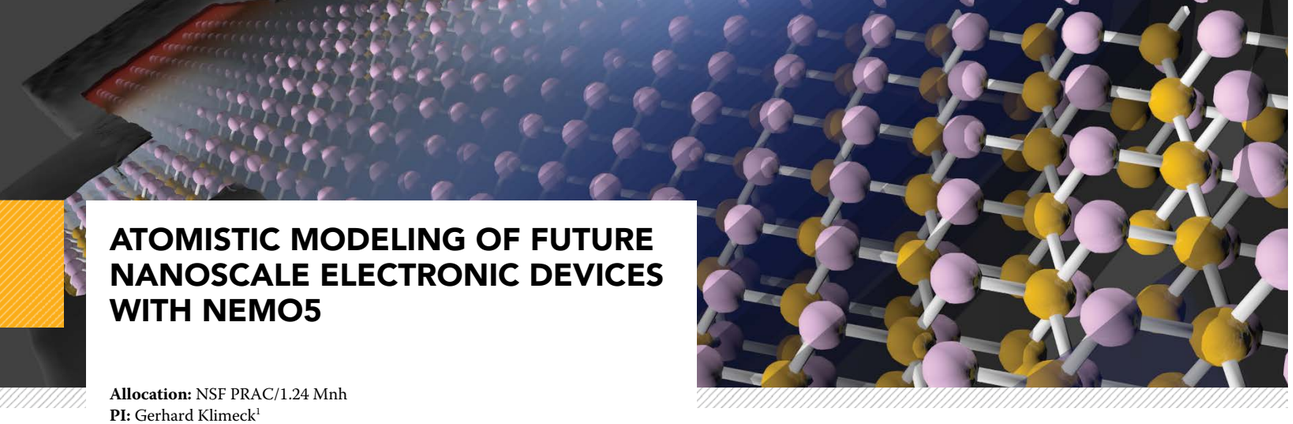

ATOMISTIC MODELING OF FUTURE NANOSCALE ELECTRONIC DEVICES WITH NEMO5

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EXECUTIVE SUMMARY:

Relentless downscaling of transistor size has continued according to Moore's law for the past 50 years. According to the International Technology Roadmap for Semiconductors, transistor size will continue to decrease in the next ten years, but foundational issues with currently unknown technology approaches must be pursued. The number of atoms in critical device dimensions is now countable. As the materials and designs become more dependent on atomic details, the overall geometry constitutes a new material that cannot be found as such in nature. The Institute for Nanoelectronic Modeling's (iNEMO) software package, NEMO5, is designed to comprehend the critical multi-scale, multi-physics phenomena through efficient computational approaches and to quantitatively model new generations of nanoelectronic devices including transistors and quantum dots, as well as to predict novel device architectures and phenomena [1,2].

FIGURE 1 (BACKGROUND): Visualization of the atomic structure and the electrostatic potential (blue/red) in a periodic ultra-thin-body device of InAs. [Credit: Daniel Mejia]

INTRODUCTION

The U.S. is a world market leader in the semiconductor industry and produces a significant number of high-paying, high-technology jobs. The U.S. semiconductor industry is one of the nation's largest export industries and the U.S. holds one-third of the global semiconductor device market worth over $300 billion. At the same time, the end of Moore's law scaling as we know it will be reached within ten years with device dimensions expected to be about 5 nm long and about five to ten atoms in its critical active device width. Further improvements in shrinking dimensions will come only through detailed study of device designs and materials and include effects such as tunneling, state quantization, and atomistic disorder.

Fundamental questions remain about the downscaling of the CMOS (complementary metal–oxide–semiconductor) switch and its eventual replacement. What is the influence of atomistic local disorder from alloy, line-edge roughness, dopant placement, and fringe electric fields? How do lattice distortions due to strain affect carrier transport in nanometer-scale semiconductor devices such as nanowires, finFETs, quantum dots, and impurity arrays? Can power consumption be reduced by inserting new materials and device concepts?

NEMO5 is developed and used by iNEMO to address fundamental questions such as those above on a variety of semiconductor devices. Besides enabling basic research covering the fields of engineering, physics, and materials science, NEMO5 is used by leading semiconductor corporations to design future devices. The source code, binaries, and support for academic use are available through nanoHUB.org.

METHODS & RESULTS

iNEMO research with the NEMO software suite on Blue Waters encompasses work for the new International Technology Roadmap for Semiconductors (ITRS) projections, disordered transistor leads, devices for quantum computing, and transistors made of materials such as bilayer graphene and topological insulators.

• NEMO5 results on future device design parameters have been included in the ITRS since 2013. Traditional device designs exploited light effective masses to increase electron mobility. Simulations showed that overall transistor characteristics can be improved by engineering a higher effective mass in order to decrease quantum tunneling and thereby reduce current leakage when devices are in the transistor OFF state.

• As devices are shrunk for performance gains, atomistic fluctuations and associated quantum effects have stronger effects on the devices' characteristics. Research into non-ideal device leads/contacts has focused on alloy disorder and how design tuning can optimize heat flow in ITRS devices to avoid Joule heating and recycle heat into usable electric power. This research showed that failure to include realistic disordered leads in simulations overestimated transistor current by a factor of two.

• Quantum dot donor configuration interaction simulations, in close collaboration with leading experimental groups, help us understand and design two-qubit gates for semiconductor quantum computing. Blue Waters simulations elucidated charging energies and the configurations of the two-electron ground state of a single negative donor as a function of depth and external electric fields. Two-electron ground states of donor molecules matched well to experimental results and a new quantum dot design has been proposed based on the electric field dependency of the exchange coupling.

• Graphene promises improved device characteristics if a suitable bandgap can be opened to provide semiconductor behavior. Recent studies with NEMO5 have simulated transport in bilayer graphene with a tight-binding approach and dynamically controlled bandgap for calibration against experimental devices.

• Surface states of topological insulator nanowires are expected to serve as scattering-free charge conductors at room temperature. The atomistic tight binding approach showed that surface state dispersion in topological insulators is geometry dependent, a result that cannot be described by simpler approaches.

WHY BLUE WATERS?

Without Blue Waters, iNEMO research is, at best, hampered, and at worst, impossible. For instance, a simple transport calculation of a 50 nm long wire with a 3 nm diameter (about 28 nm^2 in cross section) requires around 1 TFlop/s for a single energy point using the non-equilibrium Green's Function method. Resolution of a device's characteristics requires about 1,000 energy points, and this calculation must be repeated perhaps a dozen times for a full current–voltage sweep. Computational time scales with the cube of cross sectional area (relative to the direction of the electron flow) and linearly with the length of the device. The treatment of a technically currently relevant finFET device would require an atomistic resolution of a device with a cross-section around (20x40) nm^2, which includes the core semiconductor and the surrounding gate material. Blue Waters allows researchers to get results in a day, rather than weeks as on other computer systems. Additionally, some devices, such as those in the topological insulator work, are simply too large physically (due to the number of atoms and size of related tight binding matrices) to fit in memory on smaller systems.

A future generation Track-1 system would allow 100-million-atom 3D simulations for many crystals using spin and/or classical multi-physics as well as allow for ultra-scaled transistors to be simulated with important physical phenomena such as scattering and time dependence. Transistor device environments could be included, which have an increasingly strong effect on device performance as the channel region is diminished. Statistical ensembles would also be possible to investigate process and fabrication effects on physical models and on device characteristics.

Finally, Blue Waters staff provides exemplary support and user outreach to guide system usage, help with issues as they arise, and assist with code performance and scaling.

FIGURE 2: Visualization of the atomic resolved SI-Ge alloy ultra-thin-body device with surface roughness. Colors indicate source (green), drain (orange), and channel (red) regions. The grey/black area is oxide. [Credit: Daniel Mejia]